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B. E. (Fifth Semester) Examination, Nov.-Dec. 2021

(New Scheme)

(ET&T Engg. Branch)

**ADVANCED MICROPROCESSOR and
INTERFACING**

Time Allowed : Three hours

Maximum Marks : 80

Minimum Pass Marks : 28

Note : Attempt all questions. Part (a) of each question is compulsory. Attempt any two parts from (b), (c) and (d) of each unit. Draw suitable diagram whenever required.

Unit-I

1. (a) When $DT | \bar{R}$ is at logic 1, what condition does it indicate about the operation of 8086 microprocessor.

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- (b) Explain the pipelined architecture of microprocessor 8086. 7
- (c) Explain the concept of segmented memory. Also enlist its advantages. 7
- (d) Explain the following pin functions of 8086 in detail : 7
- (i) QS_0 & QS_1
 - (ii) S_0, S_1, S_2
 - (iii) Lock & TEST (active Low)
 - (iv) BHE (active Low)
 - (v) RQ | GT
 - (vi) READY
 - (vii) ALE

Unit-II

2. (a) Explain the condition for loop instruction to get terminated. 2
- (b) Define addressing modes. Discuss the various addressing modes supported by 8086 with examples. 7
- (c) Draw the interrupt structure of 8086. Explain interrupt response sequence in detail. 7

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- (d) Write an Assembly Language Program to reverse a string "ENGINEER" stored from 1000H : 2000 H & store it at 2000 H : 3000 H. 7

Unit-III

3. (a) What do you mean by COLD START. 2
- (b) Interface two $4K \times 8$ EPROMS and two $4K \times 8$ RAM chips with 8086 and select suitable maps. The address ranges are defined. 7
- EPROM \rightarrow FE000H – FFFFFH
- RAM \rightarrow FC000H – FDFFFH
- (c) Explain the Initialization sequence of 8259A. 7
- (d) Interface PIT 8254 with 8086. 8254 is interfaced at an address 0040H for counter 0. The 8254 and 8086 run at 1.5 MHz and 6 MHz respectively. Write ALPs : 7
- (i) To generate a square wave of period 1 m sec.
 - (ii) To interrupt the processor after 10 m sec.

Unit-IV

4. (a) Define bit positions of FIFO status word of 8279. 2

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PTO

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- (b) Explain how the stepper motor can be interfaced with 8086. 7
- (c) Interface ADC 0808 with 8086 using 8255 ports. Use Port A of 8255 for interfacing digital data output of ADC to the CPU and Port C for control signals. Assume that an analog I/P is present at I/P₂ of ADC and a clock Input of suitable frequency is available for ADC. Write the required ALP and Draw the schematic diagram. 7
- (d) Interface DAC 0800 with 8086 using 8255 ports. Draw the schematic & write the ALP to generate triangular wave of frequency 500 Hz. 8086 operates at 8 MHz. The amplitude of triangular wave should be +5V. 7

Unit-V

5. (a) Differentiate between interrupt & exception. 2
- (b) Draw and discuss the internal architecture of 80386. 7
- (c) Explain the paging mechanism in 80386 microprocessor. 7
- (d) Differentiate between Real, Protected and virtual mode of operation. 7